DØ Track and Preshower Trigger Level 1 Trigger Terms and Data Transfer Protocols

V07-00

Protocols for data transfers among all the elements of the DÆ Run IIa track and preshower Level 1 hardware trigger, implemented in hundreds of Field Programmable Gate Arrays, are presented along with communication protocols for all the Level 1 and Level 2 consumers of the Level 1 track and preshower trigger data as well as for the Level 3/VRB readout. Detailed descriptions of each bitfield and of numerous conventions used throughout the system are given. Also presented are all the Level 1 Trigger Terms defined by this Track and Preshower Trigger and provided to the respective Trigger Managers.

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1 LVDS Protocols for CFT/CPSax/FPS Level 1 Transfers

1.1 DFEA to CTOC

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			CR	FX	0	0	0	0	0	RA TS CFT/CPSax				L1CTT/PS DATA TYPE					L1/L2		
F2	0	0	0	HP	XPT+LC		XPT-LC			0	0		XPT+TC		XPT-TC			0	0		XPT+NC		XPT-NC			0	0	
F3	0	0	0	HP	HPT+LC		HPT-LC			0	0		HPT+TC		HPT-TC			0	0		HPT+NC		HPT-NC			0	0	
F4	0	0	0	HP	MPT+LC		MPT-LC			0	0		MPT+TC		MPT-TC			0	0		MPT+NC		MPT-NC			#PSC		
F5	0	0	0	HP	LPT+LC		LPT-LC			0	0		LPT+TC		LPT-TC			0	0		LPT+NC		LPT-NC			0	0	
F6	0	0	0	HP	SUM ABS[PT]					0	0		OL TS								ISOLATED TRACK TS							
F7/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

1.2 CTOC to CTTT

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1	1	1	1	HP	XPT+LC			XPT-LC			XPT+TC			XPT-TC			XPT+NC			XPT-NC			P/M		GI		L1/L2	
F2	0	0	0	HP	HPT+LC			HPT-LC			HPT+TC			HPT-TC			HPT+NC			HPT-NC			OL OCT				CR	FX
F3	0	0	0	HP	MPT+LC			MPT-LC			MPT+TC			MPT-TC			MPT+NC			MPT-NC	0	T1	T2	#PSC				
F4	0	0	0	HP	LPT+LC			LPT-LC			LPT+TC			LPT-TC			LPT+NC			LPT-NC			SUM ABS[PT]					
F5	0	0	0	HP	ISOLATED TRACK OCT								ISOLATED TRACK OCT								ISOLATED TRACK OCT							
F6	0	0	0	HP	OCT			RA HTPTS				0	ISOLATED TRACK OCT								ISOLATED TRACK OCT							
F7/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

1.3 DFEF to FPSS

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		0	0	0	CR	FX	0	E	W	N	S	TS FPS				L1CTT/PS DATA TYPE					L1/L2		
F2	0	0	0	HP	U	V	0	0	0	0	0	0	0	0	0	0	#PSC NO MIP				0	0	0	0	#PSC WITH MIP			
F3	0	0	0	HP	U	V	0	0	0	0	0	0	0	0	0	0	#PSC NO MIP				0	0	0	0	#PSC WITH MIP			
F4/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

1.4 FPSS to FPTT

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		0	0	0	CR	FX	0	E	W	N	S	0	0	0	0	L1CTT/PS DATA TYPE					L1/L2		
F2	0	0	0	HP	U	V	UP	LO	0	0	0	0	0	#PSC NO MIP					0	0	0	0	0	#PSC WITH MIP				
F3	0	0	0	HP	U	V	UP	LO	0	0	0	0	0	#PSC NO MIP					0	0	0	0	0	#PSC WITH MIP				
F4	0	0	0	HP	U	V	UP	LO	0	0	0	0	0	#PSC NO MIP					0	0	0	0	0	#PSC WITH MIP				
F5	0	0	0	HP	U	V	UP	LO	0	0	0	0	0	#PSC NO MIP					0	0	0	0	0	#PSC WITH MIP				
F6/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2 LVDS Protocols for CFT/CPSax/FPS Level 2 Transfers

2.1 DFEA to CTOC, L2CFT Data (*identical to DFEA to STOV/STSX*)

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC CPSax				RA TS CFT/CPSax				T	L	C	PT BIN		PT EXT			R	RA CFT H-DOUBLET							ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.2 DFEA to CTOC, L2CPSax Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	0	RA PSC CPSax				PSC WIDTH			T	L	C	PT BIN		PT EXT			R	RA TS CFT/CPSax				0	0	ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.3 CTOC to CTQD, L2CFT Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC CPSax				RA TS CFT/CPSax				T	L	C	PT BIN		PT EXT			R	RA CFT H-DOUBLET							ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.4 CTOC to CTQD, L2CPSax Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	0	RA PSC CPSax				PSC WIDTH			T	L	C	PT BIN		PT EXT			R	RA TS CFT/CPSax				0	M	ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.5 DFEA to STOV/STSX, L2STT Data (*identical to DFEA to CTOC*)

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC CPSax				RA TS CFT/CPSax				T	L	C	PT BIN		PT EXT			R	RA CFT H-DOUBLET							ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.6 STOV to STSX, L2STT Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		STOV			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC CPSax				D	RA STOV			T	L	C	PT BIN		PT EXT			R	RA CFT H-DOUBLET							ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.7 DFEF to FPSS, L2FPS Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		0	E/W	N/S	#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC FPS								PSC WIDTH			U/V	TS FPS				MIP	MIP BIT PATTERN						
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

3 G-Link Protocols for Transfers to L2 Preprocessors: L2CFT, L2PS, L2STT, and L2FPS

3.1 General Level 2 G-Link Transfer Protocol

Frame	CAV	DAV	FF	ED	Control Bits				Second Byte								First Byte							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
...	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
HF1	1	0	1	1	0	1	0	1	HEADER LENGTH								NUMBER OF OBJECTS							
HF2	1	0	1	1	0	0	0	0	HDR FORMAT				OBJECT FORMAT				OBJECT LENGTH							
HF3	1	0	1	1	0	0	0	0	CROSSING NUMBER								L2 DATA TYPE							
HF4	1	0	1	1	0	0	0	0	TURN NUMBER															
HF5	1	0	1	1	0	0	0	0	FIRMWARE MINOR VERSION								FIRMWARE MAJOR VERSION							
HF6	1	0	1	1	0	0	0	0	L2 STATUS BITS								PROCESSOR BITS							
DATA	1	0	1	1	0	0	0	0	DATA															
	1	0	1	1	0	0	0	0	DATA															
...	1	0	1	1	0	0	0	0	.....															
	1	0	1	1	0	0	0	0	.....															
TF1	1	0	1	1	0	0	0	0	L2 DATA TYPE								CROSSING NUMBER							
TF2	1	0	1	1	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP
PAD	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

3.2 CTQD to L2CFTpp, L2CFT Data

Frame	Control Bits				Second Byte								First Byte							
	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA	0	0	0	0	C	PT BIN		PT EXT			T	L	ERR CODE			R	RA PSC CPSax			
	0	0	0	0	RA CFT H-DOUBLET						ISO	0	0	TS CFT/CPSax						

3.3 CTQD to L2PSpp, L2CPSax Data

Frame	Control Bits				Second Byte								First Byte							
	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA	0	0	0	0	C	PT BIN		PT EXT			T	L	ERR CODE			R	0	0	0	0
	0	0	0	0	RA PSC CPSax				PSC WIDTH			ISO	M	TS CFT/CPSax						

3.4 DFES to L2PSpp, L2CPSst Data

Frame	Control Bits				Second Byte								First Byte							
	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA	0	0	0	0	0	PSC WIDTH			U	V	N	S	ERR CODE			0	0	0	0	0
	0	0	0	0	RA PSC CPSst								0	TS CPSst						

3.5 STSX to L2STTpp, L2CFT Data

Frame	Control Bits				Second Byte								First Byte							
	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA	0	0	0	0	C	PT BIN		PT EXT			T	L	ERR CODE			R	RA PSC CPSax			
	0	0	0	0	RA CFT H-DOUBLET						ISO	0	D	TS CFT/CPSax						

3.6 FPSS to L2FPSpp, L2FPS Data

Frame	Control Bits				Second Byte								First Byte							
	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA	0	0	0	0	MIP	MIP BIT PATTERN							ERR CODE			U/V	0	0	0	0
	0	0	0	0	RA PSC FPS								PSC WIDTH			N/S	TS FPS			

4 G-Link Protocols for Level 3 / VRB Readout

4.1 General Level 3 G-Link Transfer Protocol

Frame	CAV	DAV	FF	ED	Control Bits				Second Byte								First Byte							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
...	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
HF1	1	0	1	1	0	1	0	1	HEADER LENGTH								#DWORS MSB				#LVDS IN-LINKS			
HF2	1	0	1	1	0	0	0	0	HDR FORMAT			OBJECT FORMAT					#DWORDS LSB							
HF3	1	0	1	1	0	0	0	0	CROSSING NUMBER								L3 DATA TYPE							
HF4	1	0	1	1	0	0	0	0	TURN NUMBER															
HF5	1	0	1	1	0	0	0	0	FIRMWARE MINOR VERSION								FIRMWARE MAJOR VERSION							
HF6	1	0	1	1	0	0	0	0	L3 STATUS BITS															
DATA	1	0	1	1	0	0	0	0	DATA															
	1	0	1	1	0	0	0	0	DATA															
...	1	0	1	1	0	0	0	0	.....															
	1	0	1	1	0	0	0	0	.....															
TF1	1	0	1	1	0	0	0	0	L3 DATA TYPE								CROSSING NUMBER							
TF2	1	0	1	1	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP
PAD	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

5 FSCL Protocols for CFT/CPSax/FPS Level 1 Transfers

5.1 DFEA to L1Muon

Frame	Second Byte								First Byte							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F2	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F3	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F4	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F5	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F6	VLD	0	0	0	C	PT BIN			PT EXT			RA CFT H-DOUBLET				
F7/TF	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

5.2 CTTT or FPTT to L1 CFT/CPSax or to L1 FPS Trigger Manager

Frame	Second Byte								First Byte							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F3	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
F4	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
F5	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
F6	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
F7/TF	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

6 Explanation of Bitfields

After reviewing general terminology and definitions, description for each bitfield is given, following the bitfield name and bitlength given in square brackets. Sometimes it is necessary to further specify various bit allocations within one bitfield. In such cases, a common scheme of bit numbering is adopted in which the least significant bit is the 0^{th} bit. Both the protocols themselves (in the preceding sections) and the bitfield definitions (in the following sections) are grouped into sections according to the hardware connection to which they pertain. Within a section, bitfield definitions are ordered alphabetically. For instance, the definitions specific to the Level 1 Low Voltage Differential Signal (LVDS) transfers are given in Section 6.2, the definitions specific to the Level 2 Fiber Optic (G-Link) transfers in Section 6.4, and the definitions specific to Fast Serial Command Link (FSCL) in Section 6.6. Often the same bitfield with the same meaning appears in different hardware protocols. In such cases, its definition is given only once, in the section where it appears first. In all other sections, only the bitfield name and bitlength are repeated and a reference is given to the section where its definition appears.

6.1 Some General Terminology and Definitions

- **A Frame** is the amount of data transferred in one ~53 MHz clock cycle. Number of bits in a frame varies throughout the system. There are 28-bit LVDS frames in Level 1 or Level 2. There are 20-bit frames for G-Link transfers to L2 preprocessors (16 bits of data plus 4 the so-called outband control characters). There are 16-bit frames for FSCL transfers to the L1Muon or to the L1 CFT/CPSax and L1 FPS Trigger Managers. This means, for instance, that a STSX board receives one track's worth of data in one 28-bit LVDS frame but ships off each track on two 16-bit G-Link frames.
- **An Event Record** or simply **Record** is the amount of data a board or an FPGA receives for one physics event. For instance, the front end boards (DFEA, DFES, and DFEF) typically receive Event Records of seven 21-bit LVDS frames. As another example, CTOC board receives a variable length Event Record for L2CFT processing with a maximum length of 27 frames.
- **Note** that term **word** is generally reserved for 32-bit G-Link words in the sense used by the Level 2 and Level 3 software. This means that, for instance, one CFT track's worth of data are encoded in one 32-bit word when L1CTT/PS transmits to Level 2 preprocessors. This one 32-bit word is thus composed of two frames because it takes two ticks to transfer this amount of data, one tick per each of the two frames. This also means that, for instance, one Event Record from a CTQD board to L2CFTpp can have up to 48 data words or 48x2=96 data frames; Along the same lines,

this particular event record has 3 header words or six header frames and 1 trailer word or 2 trailer frames; And the total Event Record length in terms of frames must be divisible by 8, etc.

- Hence such commonly used terms and abbreviations as the **Begin of Record (BoR)** and the **End of Record (EoR)**.
- Whenever possible, a **transverse parity bit of a frame** and a **vertical parity frame of the event record** are provided to allow for a single-bit transmission error correction:
    - **HP [1]** — Parity of all *data* bits in the frame, i.e. horizontally, defined as "1" if the number of "1"s in the record is odd, and as "0" otherwise.
    - **VP [1]** — Parity of all *data* bits in the column of event record, i.e. vertically, defined as "1" if the number of "1"s in the column is odd, and as "0" otherwise.

  An illustration of Horizontal and Vertical parities (as well as of BoR) in a hypothetical Level 1 LVDS data transfer:

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1 / HF	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
F2	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
F3	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
F4	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
F5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
F6	0	0	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
F7 / TF	0	0	0	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	1	1	0	1	1	1	0

- Sometimes one board downstream collects identical information from several boards upstream. For instance, all DFEAs send to CTOCs the octant number (OCT) in the header. The idea behind this is that the receiving board takes majority vote on all the inputs of such particular bitfield. If a certain value is expected *a priori* (such as e.g. in case of OCT but not in case of M/P), then the correct value is always passed on and if majority vote is in disagreement an error flag is set in the readout. During intermediate stages of designs, instead of actual majority vote, such values are often taken from input Link #2, because this link carries global clock to the board in questions and therefore must always be present for board to operate.
- Unless otherwise noted, this terminology is followed throughout.

6.2 Definitions Specific to LVDS Protocols in Level 1

- **nPT±SC [3] where n = X, H, M, L** — A three bit field giving the number of tracks found in the trigger sector that meet the following conditions:
    - **nPT** — The absolute value of track p_T is between:
        - **XPT** – 10 GeV and above, MAX p_T bin;

        - **HPT** – 5 and 10 GeV, HIGH p_T bin;
        - **MPT** – 3 and 5 GeV, MEDIUM p_T bin;
        - **LPT** – 1.5 and 3 GeV, LOW p_T bin.
    - ± — The 'sign' of the track curvature, which is '+' or '–'. A positive curvature corresponds to a track that bends in the direction of increase of the azimuthal angle in D∅ coordinate system (i.e. bends counterclockwise when seen from a position along the z-axis looking North).
    - **SC** — The association of a track with the CPS cluster:
        - **NC** — tracks with no associated CPS cluster;
        - **TC** — tracks with tightly associated CPS cluster;
        - **LC** — tracks with loosely associated CPS cluster.
- **BoR [3]** — Begin of Record. Sender sets all these three bits high to indicate BoR (otherwise sets them all to low) and receiver checks if *any* two of the three bits are set high to decode BoR. Therefore, this is a single-bit self-correcting BoR marker.
- **CR [1]** — If set to "1", indicated CFT_RESET in the system. This global reset is derived from SCL's INIT/RESET signal and is passed through from Analog Front End (AFE) boards. This is critical information in terms of staying in sync with L1 Muon (from DFEAs) and with CTT Trigger Manager (from CTTT). When CR is asserted, all L1 CTT/PS transmissions to L1 Muon and to L1 CTT/PS TMs needs to be stopped. Thus, for the duration when CR is asserted, TX_ENABLE is pulled down in DFEA and in CTTT for their FSCL communications.
- **E [1]** — If set to "1", indicates East side of the FPS detectors.
- **FX [1]** — If set to "1", indicates first 'live' crossing immediately following the Sync_Gap signal, and is also derived from SCL control bits and passed through from AFEs. In absolute terms, it denotes crossing #7 in the turn. It is high for the duration of that one crossing (i.e. ~132 ns).
- **GI [1]** — Set to "1" if at least one isolated track in the octant is located in a trigger sector with occupancy below a given value.
- **HP [1]** — See Section 6.1.
- **ISOLATED TRACK OCT [8]** — Gives more detailed information on isolated track in the octant. Meanings of bits inside this 8-bit word are defined as follows:
    - **Bits [07:07]** — Set to "1" if there is an isolated track found; zero otherwise;
    - **Bits [06:04]** — Code carrying the information of the possible association of the track with the CPS axial cluster:

        - **“000”** — No association found;
        - **“001”** — Tight association with a Low CPSax cluster found;
        - **“010”** — Reserved, set to “0”;
        - **“101”** — Loose association with a Low CPSax cluster found;
        - **“110”** — Reserved, set to “0”;
    - **Bits [03:03]** — Sign of the curvature of the track, “1” for positive;
    - **Bits [02:01]** — Track p_T bin codes:
        - **“00”** — Greater than 10 GeV;
        - **“01”** — Between 5 and 10 GeV;
        - **“10”** — Between 3 and 5 GeV;
        - **“11”** — Between 1.5 and 3 GeV.
    - **Bits [00:00]** — Set to “1” if the occupancies in the ‘home’ trigger sector and in the two adjacent trigger sectors are below a given value.
- **ISOLATED TRACK TS [8]** — Gives more detailed information on isolated track in the trigger sector. Meanings of bits inside this 8-bit word are defined as follows:
    - **Bits [07:07]** — Set to “1” if there is an isolated track found; zero otherwise;
    - **Bits [06:04]** — Code carrying the information of the possible association of the track with the CPS axial cluster:
        - **“000”** — No association found;
        - **“001”** — Tight association with a Low CPSax cluster found;
        - **“010”** — Reserved, set to “0”;
        - **“101”** — Loose association with a Low CPSax cluster found;
        - **“110”** — Reserved, set to “0”;
    - **Bits [03:03]** — Sign of the curvature of the track, “1” for positive;
    - **Bits [02:01]** — Track p_T bin codes:
        - **“00”** — greater than 10 GeV;
        - **“01”** — between 5 and 10 GeV;
        - **“10”** — between 3 and 5 GeV;
        - **“11”** — between 1.5 and 3 GeV.
    - **Bits [00:00]** — Set to “1” if the occupancy in the trigger sector is below a given value.

- **LO [1]** — If set to “1”, indicates lower half of FPS detectors.
- **L1CTT/PS DATA TYPE [5]** — Defines the origin and nature of the data that follow. The codes used are single-bit self-correcting in the sense that their interpretation is correct even if one bit is in error. To distinguish between the L1 and L2 codes the **L1/L2** information must be used. The codes are:
    - **“00101”** — L1 CFT/CPSax and L2CFT;
    - **“00010”** — L1 FPS and L2FPS;
    - **“11000”** — L1 FPD and L2 CPSax;
    - **“11111”** — L2 STT.

  Receiver must check for the code above, plus for the any other five permutations of that code resulting from a single bit flips, and also the **L1/L2** bitfield to unambiguously determine one of the seven data types.
- **L1/L2 [3]** — These bits indicate whether it is ‘L1’ or ‘L2’ data. To indicate ‘L1’ data, sender sets all three bits high and receiver interprets record as ‘L1’ data if *any* two of the three bits are high. To indicate ‘L2’, sender sets all bits to low, and receiver interprets record as ‘L2’ data if *any* two of three bits are set low. In this sense, these are single-bit self-correcting codes.
- **N [1]** — If set to “1”, indicates North side of the FPS detectors.
- **OCT [3]** — CFT/CPSax octant address, a number ranging [0,7].
- **OL OCT [4]** — Measure of the 'average' fractional doublet hit occupancy of trigger sectors within an octant.
- **OL TS [8]** — Total number of ‘doublet’ hits in a trigger sector, ranging [0,240].
- **P/M [2]** — Pass and Mark codes defined as follows:
    - **“00”** — ‘Normal’ event. From the point of view of the CTT/PS firmware, a normal event is an event triggering on which is left to the Trigger Framework;
    - **“01”** — Event which carries normal data but is marked so the L1 Trigger Framework will pass it on;
    - **“10”** — This code instructs each FPGA to use an internally stored Test Vector as its input instead of the normal data input (could be propagated starting from AFEs). The Level 1 Trigger Framework will treat it as a 'Pass and Mark' event.
    - **“11”** — To be defined.
- **RA HTPTS** — Relative address within an octant of the trigger sector with the maximum **SUM ABS[Pt]**.

- **RA TS CFT/CPSax [4]** — Relative address of a trigger sector within the octant, one of ten, a number ranging [0,9].
- **S [1]** — If set to “1”, indicates South side of the FPS detectors.
- **SUM ABS[PT] [6]** — A measure of total transverse momentum of all the tracks found in a trigger sector or in an octant. A possible representation of this measure at the trigger sector level could be given by the expression

  - **SSP(k) = { SUM of ABS[Pt(i)] } / 2^n – C,**

  and at the octant level by

  - **{ SUM of SSP(k) } / 2^n – C,**

  where **n** and **C** are constants and the indices **i** and **k** refer to the track in the trigger sector and the sector within the octant, respectively. (Note that this function has not yet been implemented in the firmware.)
- **TS FPS [4]** — FPS trigger sector (φ–wedge) address for North or South side of FPS detectors, one of sixteen, a number ranging [0,15].
- **T1 [1]** — Set to “1” if at least one isolated track in the octant is loosely associated with only one CPS cluster.
- **T2 [1]** — Set to “1” if at least one isolated track in the octant is loosely associated with two CPS clusters.
- **U [1]** — If set to “1”, indicates the U orientation of preshower strips.
- **UP [1]** — If set to “1”, indicates upper half of FPS detectors.
- **V [1]** — If set to “1”, indicates the V orientation of preshower strips.
- **VP [1]** — See Section 6.1.
- **W [1]** — If set to “1”, indicates West side of the FPS detectors.
- **#PSC [2] or #PSC [3]** — A two- or three-bit field encoding total number of CPSax clusters found in a trigger sector or in an octant, respectively.
- **#PSC NO MIP [4], [5]** — A four- or five-bit field encoding total number of FPS clusters in a specified orientation (U or V) and *without* confirmation in mip layers found in a FPS trigger sector (φ–wedge) or in the half of the FPS detector, respectively.
- **#PSC WITH MIP [4], [5]** — A four- or five-bit field encoding total number of FPS clusters in a specified orientation (U or V) and *with* confirmation in mip layers found in a FPS trigger sector (φ–wedge) or in the half of the FPS detector, respectively.

6.3 Definitions Specific to LVDS Protocols in Level 2

- **BoR [1]** — See Section 6.2.

- **C [1]** — Stores information on track curvature. If a track is generated by a particle that moves in the direction of increasing azimuthal angle in D∅ coordinate system (equivalently, bends counterclockwise when viewed looking from South to North at the face of the detector), it is set to '0', otherwise it is set to '1'.
- **CROSSING NUMBER [8]** — Stores a crossing number within a turn, one of 159, ranging [1,159].
- **D [1]** — Duplicate bit for the sole usage within the STOV/STSX system. When set high indicates that the track has been sent to both neighboring STSX boards. If set low, the track has been sent to either left or right STSX board.
- **E/W [1]** — FPS East (if set to "1") or West (if set to "0") side.
- **HP [1]** — See Section 6.2.
- **ISO [1]** — Set high means that only one track is found in the trigger home-sector but no tracks are found in either of the two neighboring trigger sectors.
- **L [1]** — If set high, the track is loosely associated with a CPSax cluster. Loose track/cluster matching is not currently implemented in the firmware.
- **L1CTT/PS DATA TYPE [5]** — See Section 6.2.
- **L1/L2 [3]** — See Section 6.2.
- **M [1]** — Set high if there are more than one tracks associated with a preshower cluster.
- **MIP [1]** — Set high if any bit in **MIP BIT PATTERN** is high.
- **MIP BIT PATTERN [7]** — Seven mip bits 'in front' of the centroid of FPS cluster in a given orientation (U or V), properly offset to account for angular offset in mip versus shower layers.
- **N/S [1]** — FPS North (if set to "1") or South (if set to "0") side.
- **OCT [3]** — See Section 6.2.
- **P/M [2]** — See Section 6.2.
- **PSC WIDTH [3]** — Preshower cluster width. Binary values corresponding to cluster widths ranging [1,7]. PSC Width is set to "000" if a cluster has width greater or equal to 8 strips.
- **PT BIN [2]** — Encodes track p_T bin as follows:
    - **"00"** — MAX, $p_T > 10$ GeV;
    - **"01"** — HIGH, ~5 GeV $< p_T <$ ~10 GeV;
    - **"10"** — MEDIUM, ~3 GeV $< p_T <$ ~5 GeV;
    - **"11"** — LOW, ~1.5 GeV $< p_T <$ ~3 GeV.

- **PT EXT [3]** — The three bit 'extended' p_T field stores finer values of track p_T thresholds according to the following table:

PT BIN Name	PT BIN	EXT PT	Offset	PT min	PT max	PT average
LOW	11	111	14	-	-	-
	11	110	13	-	-	-
	11	101	12	-	-	-
	11	100	11	-	-	-
	11	011	10	-	-	-
	11	010	9	-	-	-
	11	001	8	-	-	-
	11	000	7	-	-	-
MEDIMUM	10	011	6	-	-	-
	10	010	5	-	-	-
	10	001	4	-	-	-
	10	000	3	-	-	-
HIGH	01	011	-	5.00000	5.71429	5.33333
	01	010	-	5.71429	6.66667	6.15385
	01	001	-	6.66667	8.00000	7.27273
	01	000	-	8.00000	10.00000	8.88889
MAX	00	011	-	10.00000	13.33333	11.42857
	00	010	-	13.33333	20.00000	16.00000
	00	001	-	20.00000	40.00000	26.66667
	00	000	-	40.00000	infinite	80.00000

- **R [1]** — If set high, the track is associated with a CPSax cluster outside the corresponding 4.5° trigger sector. If set low, the track is associated with a CPSax cluster in the same 4.5° trigger sector (home-sector). (In L2CPSax output of DFEA, this bit is always set to '0'.)
- **RA CFT H-DOUBLET [5]** — Relative address of a CFT H-layer doublet hit by a track. There are 44 doublets in the outermost H-layer of CFT, hence this number ranges [0,43].
- **RA PSC CPSax [4]** — Stores the relative address of the (associated) CPSax cluster centroid. There are total of 16 CPSax strips in a given CFT/CPSax trigger sector, hence the range of [0,15].
- **RA PSC FPS [8]** — Stores the address of the centroid strip of FPS cluster, one of 144, ranging [0,143].
- **RA STOV [3]** — Stores the relative address of the CFT/CPSax trigger sector where the track was found. The address is relative with respect to the STOV overlay board to which it connects. There are six trigger sectors that one STOV handles, hence the range used [0,5]. **Note** that code "111" in this bitfield is special and is reserved to encode the **Ignore** flag — tracks with this flag set will be ignored in STSX but it is useful to use this encoding for VHDL implementation purposes and is specific and internal to only STOV/STSX system.

- **RA TS CFT/CPSax [4]** — Relative address of a trigger sector within the octant, one of ten, a number ranging [0,9].
- **STOV [3]** — Encodes the number identifying one of 6 STOVs, range [0,5].
- **T [1]** — If set high, the track is tightly associated with a CPSax cluster. Note that track/cluster matching window size is dependent on track p_T and optimization of matching window was performed in D0 Note #3802.
- **TS FPS [4]** — See Section 6.2.
- **TURN NUMBER [16]** — Stores accelerator turn number.
- **U/V [1]** — Preshower strip U (if set to "1") or V (if set to "0") orientation.
- **VP [1]** — See Section 6.1.
- **#OBJ HP [2]** — Two bits each of which represents the 'horizontal' parity of **#OBJ MSB** and of **#OBJ LSB**. Refer to a table below for more details.
- **#OBJ LSB [3]** — The three least significant bits of a 6-bit number that represents total number of data frames (objects, i.e. tracks or clusters) in an event record. Note that there can be up to 24 tracks in the trigger sector or in the octant output whereas the maximum number of clusters out of a trigger sector is 8 and out of the octant is 24.
- **#OBJ MSB [3]** — The three most significant bits of a 6-bit number that represents total number of data frames (objects, i.e. tracks or clusters) in an event record.
- **#OBJ VP [3]** — Three bits representing 'vertical' parities of **#OBJ LSB** and **MSB #OBJ** when these 3-bit records are arranged in a 2x3 matrix, with top raw being **#OBJ LSB** and the bottom row being **#OBJ MSB**.
- Table Relating LSB, MSB, HP, and VP of #OBJ

LSB	**LSB(12)**	**LSB(11)**	**LSB(10)**	**HP(8)**
MSB	**MSB(15)**	**MSB(14)**	**MSB(13)**	**HP(9)**
VP	**VP(18)**	**VP(17)**	**VP(15)**	

6.4 Definitions Specific to G-Link Protocols to L2 Preprocessors

First, description of bitfields in the general L2 G-Link header and trailer is given in Section 6.4.1, followed by a description of bitfields in various L2 data words in Section 6.4.2.

6.4.1 General Level 2 G-Link Protocol

These general protocols apply to the data transfers from the L1CTT/PS system to all the relevant Level 2 preprocessors: the L2CFTpp, L2PSpp, and

L2FPSpp, all three via the VTM→FIC→MBT route, and the L2STT, via the VTM→FRC route.

- **CAV [1], DAV [1], FF [1], ED [1]** — Each of these four bits is a control bit for G-Link transmissions. All of them but DAV stay high all the time during which synchronization between sender and receiver has to be maintained. Transition from “1” to “0” on DAV indicates BoR, while transition from “0” to “1” on DAV indicates EoR.
- **Control Bits [4]** — These are the so-called G-Link outband control characters. The code ”0101” indicates the first frame, “1010” indicates the last frame, and “0000” indicates all frames in between. These control bits are made to be uniform also with the L3/VRB readout path. FIC ignores the two most significant bits of this 4-bit code. For VRB operating in the mode relevant to CTT trigger, the two least significant bits and the two most significant bits have to be identical to each other as they respectively govern/control the two 8-bit hardware buffers. FRC is going to make use of the same VRB codes for uniformity. **Note** that for the MBT purposes, the total number of frames in the event record should be divisible by 8. To accomplish this, the minimal required number of padding words is added after the vertical parity frame. This means that the EoR marker code “1010” will not necessarily appear in the vertical parity frame and can sometimes appear in the second frame of the last padding word.
- **DATA 2 x [16]** — See Section 6.4.2 for the description of bitfields in the Data Words of various L1CTT/PS to L2pp transfers.
- **FIRMWARE MAJOR / MINOR VERSION [8]** — Major / minor version number of the firmware present in a specific sender FPGA.
- **HDR FORMAT [3]** — Formatting information for the header. Presently only one code is needed for L2, so this field should be set to “001”.
- **HEADER LENGTH [8]** — The length of the G-Link header in terms of 32-bit words. It always has a value of 3.
- **L2 DATA TYPE [8]** — These codes are defined by the Level 2 for all of their inputs. The codes relevant to L1CTT/PS are:

ORIGIN DFE BOARD	L2 DATA TYPE	ORIGIN DFE BOARD	L2 DATA TYPE	ORIGIN DFE BOARD	L2 DATA TYPE
CTQD0 (CFT)	175	STSX0	181	DFES0 (CPSst)	134
CTQD1 (CFT)	176	STSX1	182	DFES1 (CPSst)	135
CTQD2 (CFT)	177	STSX2	183	DFES2 (CPSst)	136
CTQD3 (CFT)	178	STSX3	184	DFES3 (CPSst)	137
CTQD0 (CPSax)	130	STSX4	185	FPS North 0	138
CTQD1 (CPSax)	131	STSX5	186	FPS North 1	139
CTQD2 (CPSax)	132			FPS South 0	140
CTQD3 (CPSax)	133			FPS South 1	141

They will be encoded as the corresponding binary values in this 8-bit field.

- **NUMBER OF OBJECTS [8]** — Stores the total number of either tracks or clusters to be sent to the corresponding preprocessor. It is given in terms of the number of 32-bit data words, and one such word is used per track or per cluster. The total maximum number of tracks or clusters for any L1CTT/PS to L2pp communication is 48.
- **OBJECT FORMAT [5]** — Information on the version of object format. Presently, only one version of object formats exists, so this field should be set to “00001”.
- **OBJECT LENGTH [8]** — The length of each object (an object is a track or a preshower cluster data) in terms of 32-bit words. In case of L1CTT/PS sending to Level 2, it is always equal to "00000001".
- **PROCESSOR BITS [8]** — Reserved for the use by L1CTT/PS to provide any diagnostic information.
- **PAD 2 x [16]** — See the description of the **Control Bits** in this Section.
- **STATUS BITS [8]** — Defined by the Level 2 to indicate certain exceptional conditions as follows when the corresponding bit in this 8-bit word is set high:
    - **Bits [00:00]** — Monte Carlo simulated data. This means that it has to be set to “0” for all data transfers in actual hardware;
    - **Bits [03:01]** — Reserved for future use, presently set to “000”;
    - **Bits [04:04]** — Physical trailer receiver error;
    - **Bits [05:05]** — Object list truncated;
    - **Bits [06:06]** — No processing of data was attempted;
    - **Bits [07:07]** — General error condition.
- **VP [1]** — See Section 6.1.

6.4.2 Definitions Specific to Data Words in Level 2 G-Link Transfers

Definitions for most of the bitfields for L2 data words are given in Section 6.3 and so only the ones not given there are listed in this subsection.

- **ERR CODE [3]** — Reserved for encoding additional error conditions for diagnostic purposes, currently set to all zeros.
- **N [1] / S [1]** — When set to “1”, North or South CPSst strips.
- **RA PSC CPSst [8]** — Relative address of CPSst cluster within CPSst trigger sector.
- **TS CFT/CPSax [7]** — absolute address of CFT/CPSax trigger sector. There are total of 80 sectors, hence the range of [0,79].

- **TS CPSst [7]** — Code to identify CPSst trigger sectors for cluster reporting purposes only. Actual codes to be defined.
- **U [1] / V [1]** — When set to “1”, the U- or V-layer of CPSst strips.

6.5 Definitions Specific to G-Link Protocols to L3/VRB Readout

Description of bitfields in the general L3 header and trailer is given in Section 6.5.1, followed by a general description of L3 data words in Section 6.5.2.

6.5.1 General Level 3 G-Link Protocol

Historically offspring of G-Link Protocols for transfers to Level 2 pre-processors in terms of header, trailer, and all the control characters. Notable exception is abandoning concepts of Number of Objects and Object Lengths due to the fact that object length can be variable in L3/VRB transfers.

- **CAV [1], DAV [1], FF [1], ED [1]** — See Section 6.4.1.
- **Control Bits [4]** — See Section 6.4.1.
- **DATA 2 x [16]** — See the following Section 6.5.2.
- **FIRMWARE MAJOR / MINOR VERSION [8]** — See Section 6.4.1.
- **HDR FORMAT [3]** — Formatting information for the header. Presently only one code is needed for L3, so this field should be set to “010”.
- **HEADER LENGTH [8]** — The length of the G-Link header in terms of 32-bit words. It always has a value of 3.
- **L3 DATA TYPE [8]** — These codes are defined by the L1CTT/PS for all of its unique L3/VRB readouts as follows:

ORIGIN DFE BOARD	L3 DATA TYPE	ORIGIN DFE BOARD	L3 DATA TYPE	ORIGIN DFE BOARD	L3 DATA TYPE
CTOC L1	1	STSX	6	FPSS L1	8
CTOC L2CFT	2	DFES L1	7	FPSS L2	9
CTOC L2CPS	3			FPTT	10
CTTT	4			FPTT TM	11
CTTT TM	5				

  They will be encoded as the corresponding binary values in this 8-bit field.
- **OBJECT FORMAT [5]** — Information on the version of object format. Presently, only one version of object formats exists, so this field should be set to “00001”.
- **PAD 2 x [16]** — See the description of the **Control Bits** in this Section.

- **STATUS BITS [16]** — Defined by the L1CTT/PS to indicate certain exceptional conditions as follows when the corresponding bit in this 16-bit word is set high:
    - **Bits [09:00]** — One of up to 10 incoming LVDS links, numbered 0 through 9, is detected to be missing;
    - **Bits [10:14]** — Reserved for future use, presently set to “00000”;
    - **Bits [15:15]** — Logical OR of Bits [14:00].
- **#LVDS IN-LINKS [4]** — Total number of input LVDS links by design. This number is fixed for a given board, i.e. it does not change from event to event and is not affected by the number of detected missing input links on that board. Range [1,10].
- **#DWORDS MSB/LSB [4], [8]** — The two fields, MSB [4] and LSB [8], store, respectively, 4 most significant and 8 least significant bits of a 12-bit number that gives the total number of 32-bit data words (DWORDS) in the event record (i.e. the header, trailer, and padding words are not counted). Range [0,270].
- **VP [1]** — See Section 6.1.

6.5.2 Data Words in Level 3 G-Link Transfers

- **DATA 2 x [16]** — Each incoming 28-bit LVDS frame is represented by two 16-bit G-Link frames (or, equivalently, by one 32-bit G-Link word). The data sent to the L3/VRB readout is composed of blocks of event records received on input LVDS links. For instance, when the Level 1 inputs of a CTOC board are readout to L3/VRB, the data will contain first an event record received in the Level 1 time on LVDS link 0, followed by event record received on LVDS link 1 and so on. Each LVDS input frame will have to go out on two G-Link frames. This means that a 7-LVDS-frame L1 input to CTOC per LVDS link will be represented by 14 G-Link frames when readout to the L3/VRB. And there will be as many such blocks as there was input LVDS links desired to be readout to L3/VRB. When CTOC reads out its L2CFT inputs, than each such block will have a variable length of up to 27x2=54 G-Link frames (up to 24 input LVDS frames, plus 2 header and trailer frame makes maximum of 27 input LVDS frames, and when going out on G-Link a factor of 2 is introduced because each input LVDS frame has to go out on two G-Link frames).

6.6 Definitions Specific to FSCL Protocols in Level 1

FSCL (Fast Serial Copper Link) is used to communicate to L1Muon system as well as to both L1 CFT/CPSax and L1 FPS Trigger Managers. Data are sent via 16-bit frames at ~53 MHz clock. Since these are Level 1 communications,

each transmission cannot last more than 7 RF clock ticks or, equivalently, cannot have more than 7 frames in the Event Record. As a result, a unique feature of these communications is that there is no header frame. However, a vertical parity frame is still provided in the 7^{th} frame. In fact, FSCL sender itself builds and provides vertical parity of all 6 data frames, so the L1CTT/PS FPGAs do not have to provide it. Nevertheless, for standalone testing it has proved useful to have the L1CTT/PS firmware too calculate and provide the vertical parity frame in FSCL event records.

DFEA sends to L1Muon 6 highest p_T tracks in 6 FSCL frames. Bitfields in each of the 6 track frames are allocated as follows:

- **PT BIN [2]** — See Section 6.3.
- **PT EXT [3]** — See Section 6.3.
- **RA CFT H-DOUBLET [5]** — See Section 6.3.
- **C [1]** — See Section 6.3.
- **VLD [1]** — A valid bit, set to "1" if a track was found, to "0" otherwise.
- **VP [1]** — See Section 6.1.

CTTT and FPTT each send L1 CFT/CPSax and L1 FPS trigger terms (up to 96) to the respective Trigger Managers in 6 FSCL 16-bit frames. These trigger terms (or neoterms) in each subsystem are numbered 0 through 95 and their meanings are detailed in Section 7. Note that some of the neoterms are special purpose trigger terms.

7 L1CTT/PS Trigger Terms

Neoterm is a trigger detector specific Level 1 trigger term that the subsystem forms and provides to the corresponding Trigger Manager (TM) as a single bit. If the bit is set high that means that the corresponding neoterms has 'fired' according to that subsystem. One TM card can receive up to 96 neoterms (see Section 5.2) but can pass up to 32 neoterms onto Trigger Framework. There are two TM cards used in L1 CFT/CPSax subsystem and one TM card used in L1 FPS subsystem. Hence, L1 CFT/CPSax can provide up to 64 neoterms while L1 FPS can provide up to 32 neoterms. Note however that not all of these neoterms can be used for physics triggers; some of them are reserved for special purposes such as e.g. a Pass & Mark bit and certain other diagnostics. Presently, there are total of 55 L1 CFT/CPSax and 25 L1 FPS neoterms defined.

In the following subsections first all presently defined L1 CFT/CPSax and L1 FPS neoterms are described and then their mappings are given in the communications between the corresponding digital trigger term board (i.e. CTTT or FPTT) and the corresponding TM inputs (the protocols given in Section 5.2).

In the following two subsections, the L1CTT/PS neoterms, their names or 'signatures', their number (indicated in parentheses next to the name), their

meanings, parameters, and special conditions are described. All track p_T thresholds, p_T sums, etc., values are in units of GeV. A set of parameter values envisioned is listed in curly brackets. Abbreviation **psc** means preshower cluster and **trk/psc** means matched track-cluster object. When a number of required objects **n** is given, unless otherwise noted, it means that the number of those objects is required to be *equal or greater* than **n**.

7.1.1 L1 CFT/CPSax Neoterms

Presently there are following 55 L1 CFT/CPSax neoterms defined:

- **P&M (1)** — Pass and mark.
- **TTK(n,p) (8)** — CFT track or tracks as specified by the parameter values.
  - **n** — number of tracks = { 1, 2 };
  - **p** — track p_T threshold = { 1.5, 3, 5, 10 }.
- **TEL(n,p) (4)** — CFT track(s) with preshower deposition.
  - **n** — number of trk/psc = { 1 };
  - **p** — track p_T threshold = { 1.5, 3, 5, 10 };
- **TPQ(n,p,q) (8)** — Low p_T CFT track(s) with preshower deposition in a quadrant.
  - **n** — number of trk/psc = { 1, 2 };
  - **p** — track p_T threshold = { 1.5 };
  - **q** — quadrant number = { 1, 2, 3, 4 }.
- **TNQ(n,q) (8)** — Preshower cluster(s) in a quadrant.
  - **n** — number of psc = { 1, 2 };
  - **q** — quadrant number = { 1, 2, 3, 4 }.
- **TDL(n,p,s) (6)** — Pair(s) of trk/psc with same (ss), opposite (os), or ‘don’t care’ (ns) charge signs.
  - **n** — number of trk/psc = { 2 };
  - **p** — track p_T threshold = { 1.5, 5 };
  - **s** — charge sign of a pair = { ss, os, ns }.
- **TIS(n,p) (2)** — Isolated track(s).
  - **n** — number of isolated tracks = { 1 };
  - **p** — track p_T threshold = { 5, 10 }.
- **TDS(n,p,s) (2)** — Two isolated CFT tracks with same (ss) or opposite (os) charge sign.
  - **n** — number of isolated tracks = { 2 };

- **p** — track p_T threshold = { 5 };
- **s** — charge sign of a pair = { ss, os}.

- **THT(occ) (3)** — Fraction of total CFT doublet hits.
  - **occ** — average fractional occupancy in a CFT trigger sector in terms of doublet hits, i.e. average fraction of doublet hits out of 240 total number of doublets in a trigger sector, given as a percentage = { 5, 10, 20 }.
- **TAC(nsep) (2)** — Track Accoplanarity, i.e. number of sectors between two highest p_T octants (sum octant p_T > 5).
  - **nsep** — separation in terms of CFT trigger sectors, less than or greater than the specified number of trigger sectors = { lt35, gt35};
- **TIQ(n,p,q) (4)** — Isolated track(s) in a quadrant.
  - **n** — number of isolated tracks = { 1 };
  - **p** — track p_T threshold = { 5 };
  - **q** — quadrant number = { 1, 2, 3, 4 }.
- **TOC(n,p) (4)** — Octants with sum p_T above threshold.
  - **n** — number of isolated tracks = { 1, 2 };
  - **p** — sum p_T threshold = { 3, 5 };
- **TTA1 (1)** — Number of τ candidates greater or equal to one.
- **TTA2 (1)** — Number of τ candidates greater or equal to two.
- **TIL (1)** — Isolated track(s) with low home-sector occupancy.

7.1.2 L1 FPS Neoterms

Presently there are following 25 L1 CFT/CPSax neoterms defined:

- **P&M (1)** — Pass and mark.
- **FPS(n,l,side) (8)** — FPS clusters as specified by the parameter values.
  - **n** — number of clusters = { 1, 2 };
  - **l** — cluster in shower layers with or without energy deposition in mip layers, respectively ‘electron’ (el) or ‘shower’ (sh) = { el, sh };
  - **side** — North (N) or South (S) side of FPS detector = { N, S }.
- **FPQ(n,q,side) (16)** — FPS clusters per detector quadrants as specified by the parameter values.
  - **n** — number of clusters = { 1, 2 };

- **q** — FPS quadrant. The quadrants in FPS system, both North and South, are identified as East-Upper (EU), East-Lower (EL), West-Upper (WU), and West-Lower, hence = { EU, EL, WU, WL };
- **side** — North (N) or South (S) side of FPS detector = { N, S }.

7.1.3 L1 CFT/CPSax Neoterm Mapping onto the TM Inputs

The mapping of all presently defined L1 CFT/CPSax neoterms onto the bits of CTTT to Trigger Manager transfer via FSCL is given. Neoterm bit location is given as **NT[xx]** where NT stands for neoterm and xx is index to identify actual physical location of a neoterm in the L1 CFT/CPSax to Trigger Manager Event Record, it has a value 0 through 95 (the protocol is given in Section 5.2). All unused or unspecified bits are to be set to '0'.

NT[00] — P&M

NT[01] — TTK(1,1.5)
NT[02] — TTK(1,3)
NT[03] — TTK(1,5)
NT[04] — TTK(1,10)
NT[05] — TTK(2,1.5)
NT[06] — TTK(2,3)
NT[07] — TTK(2,5)
NT[08] — TTK(2,10)

NT[09] — TEL(1,1.5)
NT[10] — TEL(1,3)
NT[11] — TEL(1,5)
NT[12] — TEL(1,10)

NT[13] — TPQ(1,1.5,1)
NT[14] — TPQ(1,1.5,2)
NT[15] — TPQ(1,1.5,3)
NT[16] — TPQ(1,1.5,4)
NT[17] — TPQ(2,1.5,1)
NT[18] — TPQ(2,1.5,2)
NT[19] — TPQ(2,1.5,3)
NT[20] — TPQ(2,1.5,4)

NT[21] — TNQ(1,1)
NT[22] — TNQ(1,2)
NT[23] — TNQ(1,3)
NT[24] — TNQ(1,4)
NT[25] — TNQ(2,1)
NT[26] — TNQ(2,2)
NT[27] — TNQ(2,3)
NT[28] — TNQ(2,4)

NT[29] — TDL(2,1.5,ss)
NT[30] — TDL(2,5,ss)
NT[31] — TDL(2,1.5,os)
NT[32] — TDL(2,5,os)
NT[33] — TDL(2,1.5,ns)
NT[34] — TDL(2,5,ns)

NT[35] — TIS(1,5)

NT[36] — TIS(1,10)

NT[37] — TDS(2,5,ss)

NT[38] — TDS(2,5,os)

NT[39] — THT(5)

NT[40] — THT(10)

NT[41] — THT(20)

NT[42] — TAC(lt35)

NT[43] — TAC(gt35)

NT[44] — TIQ(1,5,1)

NT[45] — TIQ(1,5,2)

NT[46] — TIQ(1,5,3)

NT[47] — TIQ(1,5,4)

NT[48] — TOC(1,3)

NT[49] — TOC(2,3)

NT[50] — TOC(1,5)

NT[51] — TOC(2,5)

NT[52] — TTA1

NT[53] — TTA2

NT[54] — TIL

7.1.4 L1 FPS Neoterm Mapping onto the TM Inputs

The mapping of all 25 presently defined L1 FPS neoterms onto the bits of FPTT to Trigger Manager transfer via FSCL is given. Neoterm bit location is given as **NT[xx]** where NT stands for neoterm and xx is index to identify actual physical location of a neoterm in the L1 FPS to Trigger Manager Event Record, it has a value 0 through 95 (the protocol is given in Section 5.2). All unused or unspecified bits are to be set to '0'.

NT[00] — P&M

NT[64] — FPS(1,el,S)

NT[65] — FPS(2,el,S)

NT[66] — FPS(1,sh,S)

NT[67] — FPS(2,sh,S)

NT[68] — FPS(1,el,N)

NT[69] — FPS(2,el,N)

NT[70] — FPS(1,sh,N)

NT[71] — FPS(2,sh,N)

NT[80] — FPQ(1,WU,S)

NT[81] — FPQ(2,WU,S)

NT[82] — FPQ(1,WL,S)

NT[83] — FPQ(2,WL,S)

NT[84] — FPQ(1,EU,S)

NT[85] — FPQ(2,EU,S)

NT[86] — FPQ(1,EL,S)

NT[87] — FPQ(2,EL,S)

NT[88] — FPQ(1,WU,N)

NT[89] — FPQ(2,WU,N)

NT[90] — FPQ(1,WL,N)

NT[91] — FPQ(2,WL,N)

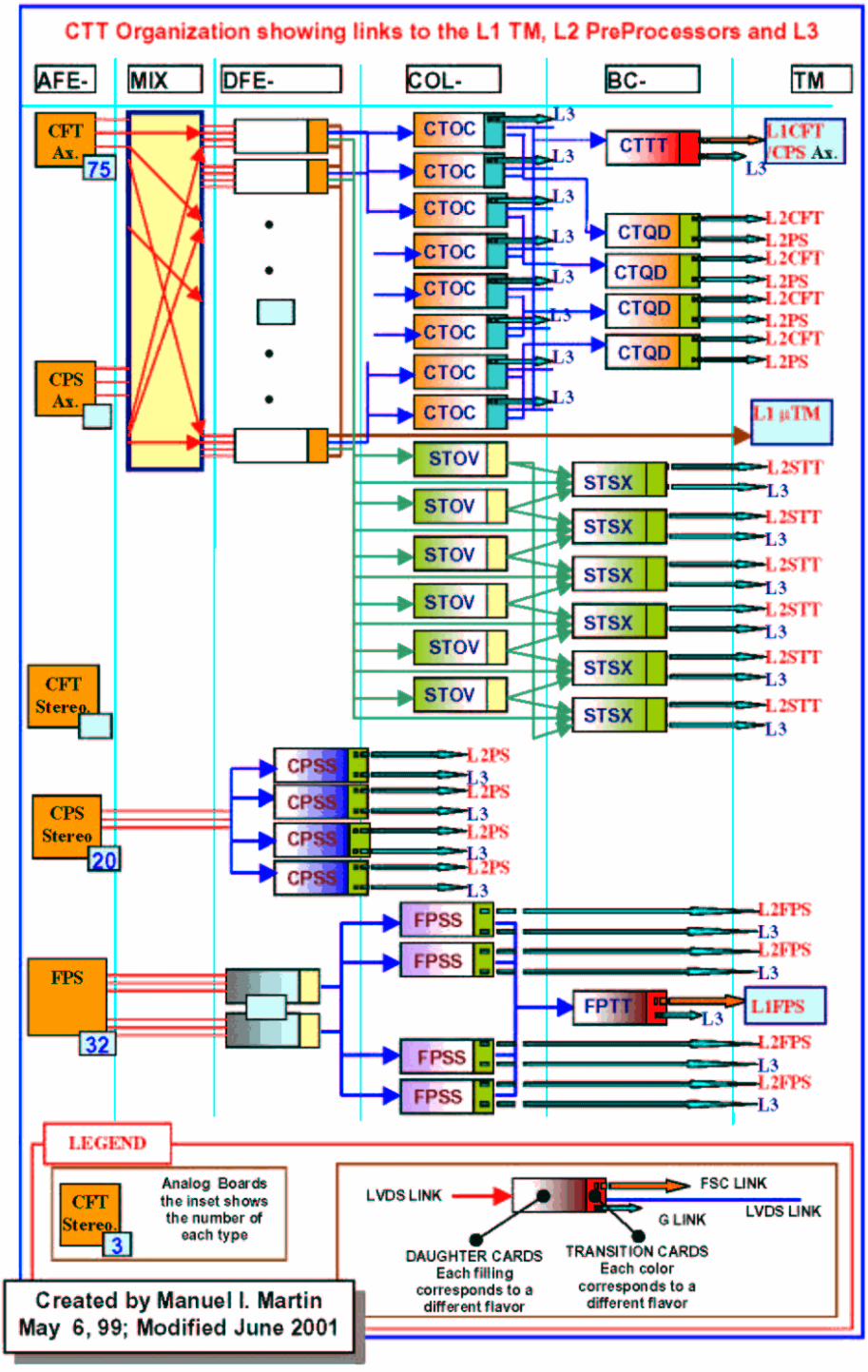
NT[92] — FPQ(1,EU,N)

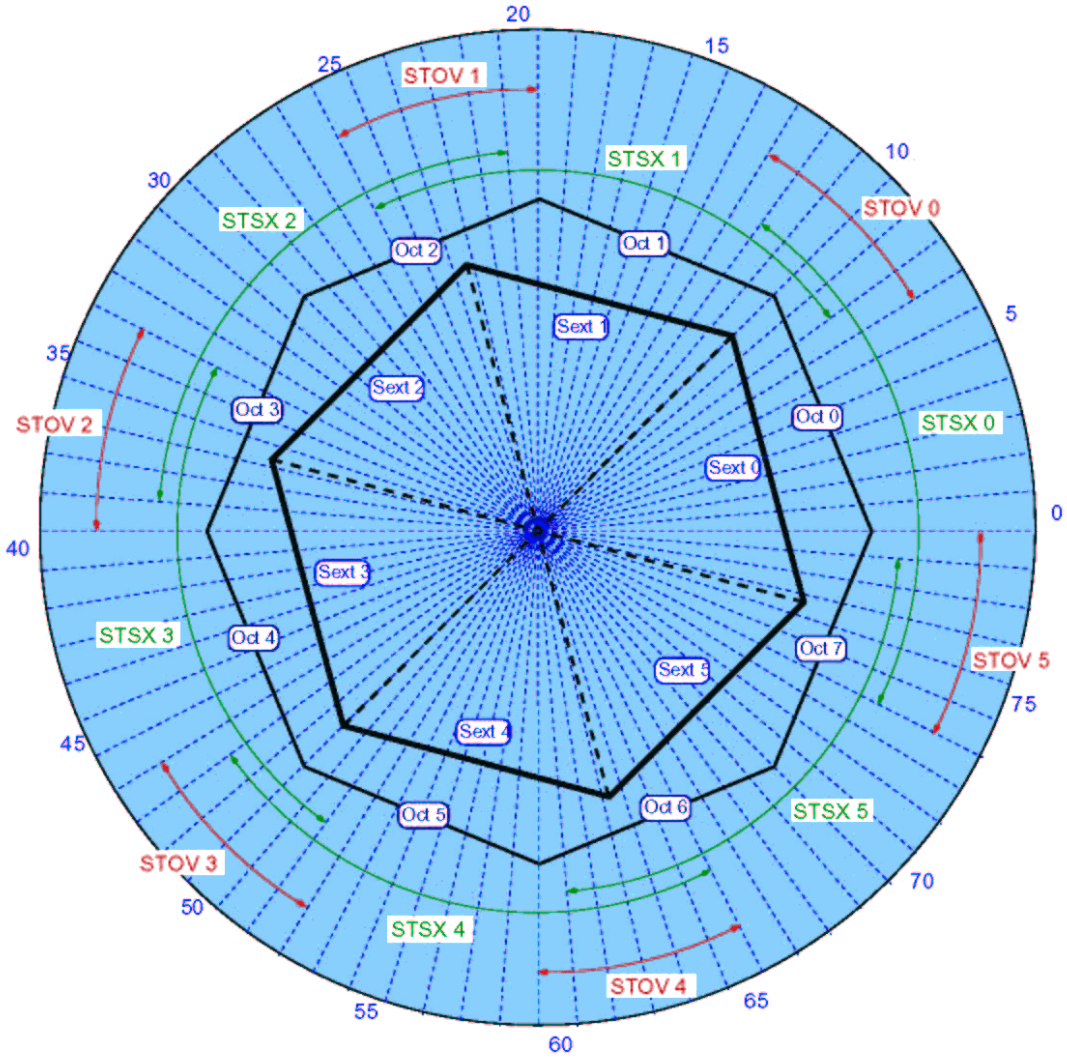
NT[93] — FPQ(2,EU,N)

NT[94] — FPQ(1,EL,N)

NT[95] — FPQ(2,EL,N)

8 System Architecture

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STOV 1
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STOV 0
STSX 2
STSX 0
STOV 2
STOV 5
STSX 3
STSX 5
STOV 3
STSX 4
STOV 4
Oct 1
Oct 2
Oct 0
Oct 3
Oct 7
Oct 4
Oct 6
Oct 5
Sext 1
Sext 2
Sext 0
Sext 3
Sext 5
Sext 4